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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,240	SHIN, SOON-KYUN	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10-17,19-29,32 and 33* is/are rejected.

7)☒ Claim(s) *5-9,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to papers filed 2/28/06. The rejection in previous office action is maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 17, 26-28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Pan (USP 6734718).

As to claims 1 and 17, Pan's figure 4 shows an apparatus for controlling a boosted voltage, comprising: a voltage generating circuit (circuit figure 4) configured to generate a boosted voltage (Vn) from an input voltage (V0) based on a control current (output of 450) and charges stored in a charge storing element (it is inherent that capacitors are in elements 410-430, see figures 2 and 6) and configured to receive the control current while the charges stored in the charge storing element are used to generate the boosted voltage; the voltage generating circuit include, a clock signal generator (inherent, see figures 2, 6 and 7); a level shifter circuit (410, 420) selectively changing a level of the input voltage based on a clock signal output from the clock signal generator, and a switching structure (the transistors in figure 7) configured to selectively store the charges in the charge storage element and selectively output the stored charges in conjunction with charges corresponding to the control current as the boosted voltage

based on output from the clock signal generator and the level shifter circuit; and a control circuit (450) configured to generate the control current based on the boosted voltage.

As to claim 2, figure 4 shows that the voltage generating circuit comprises: a capacitor (se figures 2 and 6); and the switching structure is configured to selectively store charges corresponding to the input voltage in the capacitor, and to selectively output the stored charges in conjunction with charges corresponding to the control current as the boosted voltage.

As to claim 26, Pan's figures 4 and 7 show that the switching structure is configured to selectively receive the control current while configured to selectively output the stored charges.

As to claim 27, Pan's figures 2, 4 and 7 show that the switching structure includes a switch configured to selectively connect a portion of the control circuit generating the control current with the capacitor.

As to claim 28, figures 2, 4 and 7 show that the voltage generating circuit is configured to not receive the control current when charges are stored in the capacitor (when T3 is off).

Claim 32 recites similar limitations of claim 1. Therefore, it is rejected for the same reasons.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 10-16 and 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (USP 6734718) in view of Bayer et al. (USP 6392904) (previously cited).

As to claim 3, Pan's figure 4 shows all elements except for the detail of the voltage detector circuit. However, Bayer et al.'s shows a circuit having voltage detector (R1, R2, 9, 5, Rk, Ck). It would have been obvious to one having ordinary skill in the art to use Bayer et al.'s voltage detector for Pan's voltage detector for the purpose of providing a precise desired output voltage VN. Thus, the modified Pan's figure 4 shows that the control circuit is configured to generate the control current based on a difference between the boosted voltage and a desired boosted voltage (output of Bayer et al.'s voltage source 9).

As to claim 10, the modified Pan's figure 4 shows that the control circuit is configured to generate the control current based on the boosted voltage and a desired boosted voltage.

As to claim 11, the modified Pan's figure 4 shows that the control circuit is configured to generate the control current based on a difference between the boosted voltage and the desired boosted voltage

As to claims 12 and 14, the modified Pan's figure 4 shows that the control circuit comprises: a voltage divider (Bayer et al.'s R1, R2) configured to generate a divided voltage from the boosted voltage; a comparator/amplifier (Bayer et al.'s 5) configured to compare the divided voltage with a reference voltage (9); and a current generator (Pan's T1, T2 in figure 7) configured to generate the control current based on output from the comparator.

As to claims 13 and 15, the modified Pan's figure 4 shows that the reference voltage represents a desired boosted voltage.

As to claim 16, the modified Pan's figure 4 shows that voltage controlled current source decreases the control current when the divided voltage is higher than the reference voltage, and increases the control current when the divided voltage is lower than the reference voltage.

Claims 19-25 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

5. Claims 4 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over St. Pierre (USP 6208196) in view of Pan (USP 6734718).

As to claim 4, St. Pierre's figure 1 shows a boosted voltage generator comprising a charge storage device (C2); level shifter (C1, M1); clock signal generator (circuit, not shown, that generates CLK and INV3); and switch structure (M2 and INV1). Thus, figure 1 shows all elements of the claim except for the switch structure is responsive to the control current circuit. However, Pan's figure 4 shows a boosted voltage generator having a control current circuit (450, 460) for controlling the driver figure 7 in order to reduce ripple. Therefore, it would have been obvious to one having ordinary skill in the art to use Pan's current control circuit to control St. Pierre's driver INV1 for the purpose of reducing ripple. Thus, the modified St. Pierre further shows that the switching structure includes first, second, third and fourth switches (Pan's T3 and T4 in Pan INV2 and St. Pierre's M2, M3); and the voltage generating, circuit further comprises: a capacitor (St. Pierre' s C2) configured to store charges corresponding to the input voltage while the second and third switches are turned on, and outputting the boosted voltage while the first and fourth switches are turned on.

As to claim 29, the modified St. Pierre's figure 1 shows that the first switch is configured to connect a portion of the control circuit generating the control current with the capacitor when turned on.

Response to Arguments

6. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that "the current control circuit 450 of Pan does not output a "control current," but instead, only outputs a clock signal CLK to control the current output from the voltage multiplier stages 410, 420 and 430". The Examiner respectfully disagrees. Pan's figure 7 shows that the current control circuit generates two signals, clock signal and signal coupled to the gate of T1. As shown in figure 7, transistors T1 and T2 determine current going through inverter (T3 and T4). Thus, the signal that coupled to the gate of transistor T1 is a current control signal.

Allowable Subject Matter

7. Claims 5-9, 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 33 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 5-9, 30 ad 31 would be allowable because the prior art fails to teach or suggest the first and second switches are switched in response to first and second clock signals.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

April 3, 2006